UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte UDO WALTERSCHEIDT and THOMAS E. WILLIS

Appeal No. 2006-0537
Application No. 09/753,766

ON BRIEF

Before THOMAS, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 through 19.

Representative claim 1 is reproduced below:

1. A multi-threading processor, comprising:

a front end module;

an execution module coupled to said front end module;

a state module coupled to said front end module and said execution module; and

a switch logic module coupled to said state module, wherein said switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch.

The following references are relied on by the examiner:

Bondi et al. (Bondi)	5,881,277	Mar. 09, 1999
Parady	5,933,627	Aug. 03, 1999
Borkenhagen et al. (Borkenhagen)	6,567,831	May 20, 2003

Claims 1-19 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Parady in view of Bondi as to claims 1 through 4, 6 through 9, 14 and 15, with the addition of Borkenhagen as to claims 5, 10 through 13 and 16 through 19.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief (no reply brief has been filed) for the appellants' positions, and to the answer for the examiner's positions.

OPINION

Based upon the extensive analysis, set forth in the examiner's rather lengthy, well-reasoned answer, we sustain the rejections of all claims on appeal under 35 U.S.C. § 103, as embellished upon here.

At the outset, we note that pages 3 through 10 of the brief set forth arguments only as to independent claims 1, 8 and 14 as well as dependent claims 2, 3 and 4 in the first stated rejection. On the other hand, as to the second stated rejection, appellants indicate at the bottom of page 10 of the brief that the rejection of the noted dependent claims must fail because of the above-noted deficiencies with respect of the combination of Parady and Bondi as to the

first stated rejection. Thus, appellants only argue here their parent independent claims in the first stated rejection. Correspondingly, there are no arguments presented to us that the additional reference to Borkenhagen is not properly combinable within 35 U.S.C. § 103 with Parady and Bondi and does not argue against what the examiner's says Borkenhagen teaches.

We agree with the examiner's initial statement of the rejection at pages 3 through 9 of the answer, which has been embellished extensively by the correlation of each of the cited features of claims 1 through 4 in tabular form at pages 9 through 17 of the answer. Additionally, the examiner has correlated in tabular form the features of independent claims 1, 8, and 14 at pages 17, 26 and 27 of the answer. These correlations are compelling of the obviousness of the claimed subject matter of the argued claims.

The arguments presented in the brief beginning at page 3 have been specifically addressed by the examiner beginning at page 18 in the Responsive Arguments portion of the answer. From our point of view, these arguments are equally unpersuasive of patentability. We note initially as to independent claim 1 that the claimed front end module, the execution module, and the state module have no stated functions recited for them. The comparison of appellants' Figure 1 with Figure 3 of Paraday at pages 4 and 5 of the brief is equally unpersuasive. All of the elements of the specification Figure 1 at page 4 of the brief are not

specifically recited in independent structure claim 1 on appeal. Appellants' arguments appear to invite us to read all of the details shown in Figure 1 into the subject matter of claim 1 on appeal. The claimed SoEMT processor of specification Figure 1 appears to be substantially a prior art device as noted at the top of the specification page 2. As well discussed by the examiner, the claimed "coupled to" language in this claim does not require a direct connection between the recited element "but only some type of connection so data can travel from point A to point B" as discussed at the bottom of page 21 of the answer. In terms of the "comprising" language utilized as the basis for the connective between the preamble and the body of claim 1 on appeal, appellants rightly note at the top of page 6 that this is open-ended claim language. The examiner additionally correctly notes, however, that there "is no limitation in the word 'coupled' as to the number of elements the data can travel through before reaching its destination as long as the data reaches its destination."

We likewise disagree with appellants' urging at the top of page 7 of the brief that the thread switching logic 112 in Parady's Figure 3 does not detect a long-latency event. At a minimum, we consider that the artisan would have considered this capability as a trigger event, therefore, as a kind of detection of the event. Parady has consistently taught that the switching logic 112 functions "in response to long-latency events" as expressed initially in the abstract of

Parady's patent. Correspondingly, Bondi's Figure 3 execute unit 52 appears to detect misdirected branch instructions as claimed, thus activating a proper fetch in instruction fetch unit 38.

As to the motivation issue, we recognize as well as the examiner admitting that Parady does not even mention and is not specifically concerned with the problem of latency of mispredicted branches per se. Appellants' argument at page 8 of the brief that without the benefit of the present application, "one skilled in the art would only be motivated to add Bondi's reduced latency mispredicted branches to Parady's system, resulting in a system with both performance improvements" appears to admit the proper combinability of these two references.

Correspondingly, the examiner's best statement of the combinability issue appears to be expressed at pages 19 and 20 of the answer which we reproduce here, and which is somewhat repeated beginning at page 24:

> Parady has taught that switch logic module detects a long latency event in a software thread and schedules a switch to another software thread during a latency of said long latency event (Parady column 2, lines 18-19 and column 2, lines 27-29). Parady has even taught that jump instructions, which are equated to branch instructions (InstantWeb's Free On-line Computing Dictionary 'branch'), are long latency instructions (Parady column 4, lines 6-8). Parady has not taught that 'branch misprediction' is one of his set of long-latency events. Bondi has taught that branch misprediction requires 'numerous cycles...to reset the pipeline(s) to an operational state and, thus, valuable processor cycle time is lost.' In essence, Bondi has taught that a branch misprediction is a long

> latency event, since it requires numerous cycles to resolve, and it is 'one of the more serious impediments to realizing even higher processor performance (Bondi column 1, lines 62-64).' Parady has taught that a thread switch occurs on a long latency event (see above) and multi-threading reduces the impact of long latency events (Parady column 1, lines 58-59). A person of ordinary skill in the art would have recognized that a branch mispredict is a type of long latency event and reducing the performance penalty due to the misprediction would increase processor performance. Therefore, it would have been obvious to modify Parady to switch threads on a branch misprediction in order to reduce the performance penalty suffered by the misprediction. The test of obviousness is not what has been taught explicitly by each reference, as suggested by Applicant's arguments, but what the two references suggest to a person of ordinary skill in the art at the time the invention was made (In re Bozek, 163 USPQ 545 (CCPA 1969) 'The test for obviousness is not whether the features of one reference may be bodily incorporated into the other to produce the claimed subject matter by simply what the combination of references makes obvious to one of ordinary skill in the pertinent art.'; In re Van Beckum, 169 USPQ 47 (CCPA 1971) 'We would note that it is well settled that the test of obviousness is not whether the features of one reference can be bodily incorporated in to the structure of another and proper inquiry should not be limited to the specific structure shown by the references, but should be into the concepts fairly contained therein, and the overriding question to be determined is whether those concepts would suggest to one skilled in the art the modifications called for by the claims.', In re Sheckler, 168 USPQ 716 (CCPA 1971) '...It is, of course, not necessary that either Barnes or Dryden actually suggest, expressly or in so many words, the changes or possible improvements appellant has made').

As noted by the examiner, the teaching at column 4, lines 6 through 8 of Parady indicates that his invention "could be added to other potentially long-latency operations, such as jump instructions." These jump instructions are

branch instructions as specifically discussed in a brief paragraph bridging columns 4 and 5 of Parady as well. As to Bondi, the pipeline nature of Bondi's invention corresponds to the pipeline processors 32 through 46 of Parady's Figure 1 which are depicted as element 41 in Figure 3 and the various execution units in Figures 5 and 6. Correspondingly, Bondi's instruction pipeline operates on program thread information in the same manner that Parady's processors do.

In view of the foregoing, the decision of the examiner rejecting claims 1 through 19 on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS)
Administrative Patent Judge)
)
JOSEPH F. RUGGIERO) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
HOWARD B. BLANKENSHIP)
Administrative Patent Judge)

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Kenyon & Kenyon
Suite 600
333 W. San Carlos Street
San Jose, CA 95110-2711